IN THE CLAIMS:

1. (cancelled)

2-5. (previously cancelled)

6. (currently amended) A data processor on a semiconductor substrate, comprising:

an electrically erasable or programmable non-volatile program memory;

a central processing unit capable of accessing the non-volatile program memory; and

a control circuit;

wherein the data processor operates in a boot mode;

wherein the control circuit terminates ~~terminating~~ a process for erasing or programming of data in the program memory in response to an interrupt request or an exception processing request to the central processing unit during erasing or programming of the data in the program memory in the boot mode; and

wherein in the boot mode the data processor operates in part to input data from outside the semiconductor substrate for programming in the program memory ~~in accordance with a request for erasing or programming the data in the program memory~~.

7. (currently amended) A data processor formed on a semiconductor substrate, comprising:

an electrically erasable or programmable non-volatile program memory;

a central processing unit capable of accessing the non-volatile program memory; and

a control circuit excluding an interrupt request or an exception processing request to the central processing unit during erasing or programming of data in the non-volatile program memory in accordance with a request for erasing or programming the data in the non-volatile program memory in a boot mode;

wherein in the boot mode the data processor operates in part to input data for programming into the non-volatile program memory.

8. (new) A data processor according to claim 6, wherein an interface circuit of the data processor inputs data for programming in the program memory in the boot mode.

9. (new) A data processor according to claim 7, wherein an interface circuit of the data processor inputs data for programming in the non-volatile program memory in the boot mode.